AMENDMENTS TO THE CLAIMS

This listing of the claims will replace all prior versions and listings of claims in the application:

Listing of Claims

1. (currently amended) A method of configuring a memory controller, said memory controller having a plurality of input/output pins, said method comprising:

informing said memory controller of a type of memory; and

configuring at least one of said ~~pin~~ pins to have a functionality in accordance with said type of memory, said functionality including control, chip select, and clock functions.

2. (original) The method of claim 1 wherein said type of memory is a buffered memory.

3. (original) The method of claim 1 wherein said type of memory is an unbuffered memory.

4. (original) The method of claim 1 wherein said configuring comprises configuring said functionality of said pin to a clock signal function.

5. (original) The method of claim 4 wherein said clock signal function is a differential clock signal function.

6. (original) The method of claim 1 wherein said configuring comprises configuring said functionality of said pin to a chip select signal function.

7. (currently amended) The method of claim 1 wherein said functionality of said pin is one of a chip select signal ~~function~~ and a clock signal ~~function~~.

8. (original) A method of providing more than one function for an output pin of a memory controller, said method comprising:

providing a clock signal within said memory controller;

providing a control signal within said memory controller;

selecting within said memory controller one of said clock signal and said control signal based on a type of memory; and

coupling said selected signal to said output pin.

9. (original) The method of claim 8 wherein said type of memory is a buffered memory.

10. (original) The method of claim 8 wherein said type of memory is an unbuffered memory.

11. (original) The method of claim 8 wherein said clock signal is a differential clock signal.

12. (original) The method of claim 8 wherein said control signal is a chip select signal.

13. (original) A memory controller comprising:

at least one output pin;

a multiplexer having two inputs, a control input, and an output coupled to said output pin;

a chip select signal coupled to one of said two inputs;

a control signal coupled to the other one of said two inputs; and

a signal coupled to said control input that selects one of said chip select signal and said control signal based on a type of memory.

14. (original) The memory controller of claim 13 wherein said type of memory is a buffered memory.

15. (original) The memory controller of claim 13 wherein said type of memory is an unbuffered memory.

16. (currently amended) ~~The~~ A memory controller ~~of claim 13 wherein said control signal is~~ comprising:

at least one output pin;

a multiplexer having two inputs, a control input, and an output coupled to said output pin;

a chip select signal coupled to one of said two inputs;

a clock signal coupled to the other one of said two inputs; and

a signal coupled to said control input that selects one of said chip select signal and said clock signal based on a type of memory.

17. (original) The memory controller of claim 16 wherein said clock signal is a differential clock signal.

18. (original) A memory controller comprising:

at least one output pin;

a multiplexer having two inputs, a control input, and an output coupled to said output pin;

a clock signal coupled to one of said two inputs;

a control signal coupled to the other one of said two inputs; and

a signal coupled to said control input that selects one of said clock signal and said control signal based on a type of memory.

19. (original) The memory controller of claim 18 wherein said type of memory is a buffered memory.

20. (original) The memory controller of claim 18 wherein said type of memory is an unbuffered memory.

21. (original) The memory controller of claim 18 wherein said control signal is a chip select signal.

22. (original) The memory controller of claim 18 wherein said clock signal is a differential clock signal.

23. (currently amended) A memory controller comprising:

at least one output pin; and

circuitry coupled to said output pin that provides said output pin with selectable functionality in accordance with a type of memory, said functionality including control, chip select, and clock functions.

24. (currently amended) The memory controller of claim 23 wherein said functionality of said output pin is one of a chip select signal ~~function~~ and a clock signal ~~function~~.

25. (currently amended) A memory circuit comprising:

a plurality of memory modules, said memory modules being of at least one type; and

a memory controller coupled to said memory modules via a plurality of pins, at least one of said pins having a selectable functionality based on said type of said memory modules, said functionality including control, chip select, and clock functions.

26. (currently amended) The memory circuit of claim 25 wherein said selectable functionality comprises a clock signal ~~function~~.

27. (currently amended) The memory circuit of claim 25 wherein said selectable functionality comprises a chip select signal ~~function~~.

28. (currently amended) A computer system comprising:

a central processing unit;

a memory controller coupled to said central processing unit, said memory controller having a plurality of input/output pins; and

a plurality of memory modules of at least one type coupled to said memory controller via said pins; wherein:

a ~~subplurality~~ subset of said pins has selectable functionality, said functionality based on said

type of said memory modules, said functionality including control, chip select, and clock functions.

29. (currently amended) The computer system of claim 28 wherein said selectable functionality comprises a clock signal ~~function~~.

30. (currently amended) The computer system of claim 28 wherein said selectable functionality comprises a chip select signal ~~function~~.

31. (currently amended) Apparatus for configuring a memory controller, said memory controller having a plurality of input/output pins, said apparatus comprising:

means for informing said memory controller of a type of memory; and

means for configuring at least one pin of said memory controller to have a functionality in accordance with said type of memory, said functionality including control, chip select, and clock functions.

32. (original) Apparatus for providing more than one function for an output pin of a memory controller, said apparatus comprising:

means for providing a clock signal within said memory controller;

means for providing a control signal within said memory controller;

means for selecting within said memory controller one of said clock signal and said control signal based on a type of memory; and

means for coupling said selected signal to said output pin.

33. (original) A memory controller comprising:

at least one output pin;

multiplexer means for outputting one of at least two signals to said output pin;

signal means for selecting a chip, said signal means coupled to said multiplexer means;

control signal means coupled to said multiplexer means; and

means coupled to said multiplexer means for selecting said control signal means based on a type of memory.

34. (original) A memory controller comprising:

at least one output pin;

multiplexer means having two inputs, a control input, and an output coupled to said output pin;

a clock signal coupled to one of said two inputs;

a control signal coupled to the other one of said two inputs; and

means coupled to said control input for selecting one of said clock signal and said control signal based on a type of memory.

35. (currently amended) A memory controller comprising:

at least one output pin; and

means for providing said output pin with selectable functionality in accordance with a type of memory,

said functionality including control, chip select, and clock functions.

36. (currently amended) A memory circuit comprising:

a plurality of memory modules, said memory modules being of at least one type; and

memory controller means coupled to said memory modules via input/output means, at least some of said input/output means having a selectable functionality based on said type of said memory modules, said functionality including control, chip select, and clock functions.

37. (currently amended) A computer system comprising:

central processing means;

memory controller means coupled to said central processing means, said memory controller means having a plurality of input/output means;

a plurality of memory modules of at least one type coupled to said memory controller means via said input/output means; wherein:

a ~~subplurality~~ subset of said input/output means has selectable functionality, said functionality based on said type of said memory modules and including control, chip select, and clock functions.